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Data Movement under the von Neumann Computer Architecture

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Abstract: Big data applications have changed the landscape of computing. A most fundamental question today is how to design a data-centric computer architecture for the big data era. The traditional von Neumann architecture is computing centric. The known dataflow architecture is also computing centric where data flow is arranged to maximize parallel computations. In this study, we first reexamine computer architectures from a data-centric point of view. We find von Neumann preserves a neutrality between computing and memory. The traditional compute-centric focus of von Neumann is due to historical reasons. We next reexamine memory systems of von Neumann from a data-centric point of view and introduce several metrics and methods to model and optimize memory systems. We then extend the memory system analysis to computing and to the trade-off between computing and data movement. Finally, we propose the data flow under von Neumann computer architecture approach, noted as dataflowV. DataflowV determines where and how to conduct computing with the consideration of data movement cost. DataflowV is not a new computer architecture. It is a data-centric implementation of the von Neumann computer architecture. We model memory systems performance using four different types of memory cycles. Through an in-depth, hierarchical analysis of these four types of memory cycles and computing cost, we have formulated the trade-off of computing and data movement. While dataflowV is a challenge task, any of its "point solutions" can benefit current computing systems immediately. We will present the concept, modeling, and design of dataflowV and some of its implementation results in this talk. We will also discuss research issues related to dataflowV and memory systems in general

Bio: Dr. Xian-He Sun is a University Distinguished Professor and the Ron Hochsprung Endowed Chair of Computer Science at the Illinois Institute of Technology (Illinois Tech). Before joining Illinois Tech, he worked at DoE Ames National Laboratory, at ICASE, NASA Langley Research Center, at Louisiana State University, Baton Rouge, and was an ASEE fellow at Navy Research Laboratories. Dr. Sun is an IEEE fellow and is known for his memory-bounded speedup model, also called Sun-Ni's Law, for scalable computing. His research interests include high-performance computing, memory and I/O systems, and performance evaluation and optimization. He has over 300 publications, 6 patents in these areas, and is currently leading two multi-institution large NSF software development projects. He is an Associate Editor-in-Chief of the IEEE Transactions on Parallel and Distributed Systems, and a former chair of the Computer Science Department at Illinois Tech. He received the Golden Core award from the IEEE CS society in 2017, the ACM Karsten Schwan Best Paper Award in 2019, and the first prize best paper award from CCGrid in 2021. More information about Dr. Sun can be found at his web site www.cs.iit.edu/~sun/.